

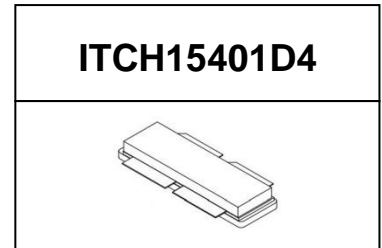


1300-1500MHz, 400W, High Power RF LDMOS FETs

Description

ITCH15401D4 is a 400-watt, internally matched LDMOS FETs, designed for multiple applications with frequencies from 1300-1500MHz

- Typical Performance (on Innegration fixture with device soldered):
V_{dd}=28V, V_{gs}=2.26V, I_{dq}=40mA, T_c=25 degree C, Test signal: CW,



Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	Id(A)	Gp(dB)	Eff
1300	40.6	56.0	400	22.5	15.4	63.5%

Features

- Low cost, high reliable solution.
- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	65	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+32	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _{case} = 85°C, T _j = 200°C, DC Power supply	R _{θJC}	0.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Breakdown Voltage (V _{GS} =0V; I _D =100uA)	V _{DSS}	65	---	---	V
Zero Gate Voltage Drain Leakage Current	I _{DSS}	---	---	10	μA



($V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$)					
Gate--Source Leakage Current ($V_{GS} = 6\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	---	---	1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{ V}$, $I_D = 600\text{ }\mu\text{A}$)	$V_{GS(th)}$	---	1.6	---	V
Gate Quiescent Voltage ($V_{DD} = 28\text{ V}$, $I_{DQ} = 40\text{ mA}$, Measured in Functional Test)	$V_{GS(Q)}$		2.26		V

Functional Tests (In Innegration 1.3GHz Test Fixture, 50 ohm system) : $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 40\text{ mA}$, $f = 1300\text{ MHz}$, Pulse CW Signal Measurements. Pulse width:100uS,Duty cycle:10%, Pin=10W

Power Gain	G_p	---	16	---	dB
Drain Efficiency@Pout	η_D		63	---	%
Output Power	Pout	350	400	---	W
Input Return Loss	IRL	---	-7	---	dB

Figure 1: Gain and Efficiency as function of output power

Signal: Pulse width 100us, duty cycle 10% , $V_{GS} = 2.26\text{ V}$, $V_{DD} = 28\text{ V}$, $I_{DQ} = 40\text{ mA}$

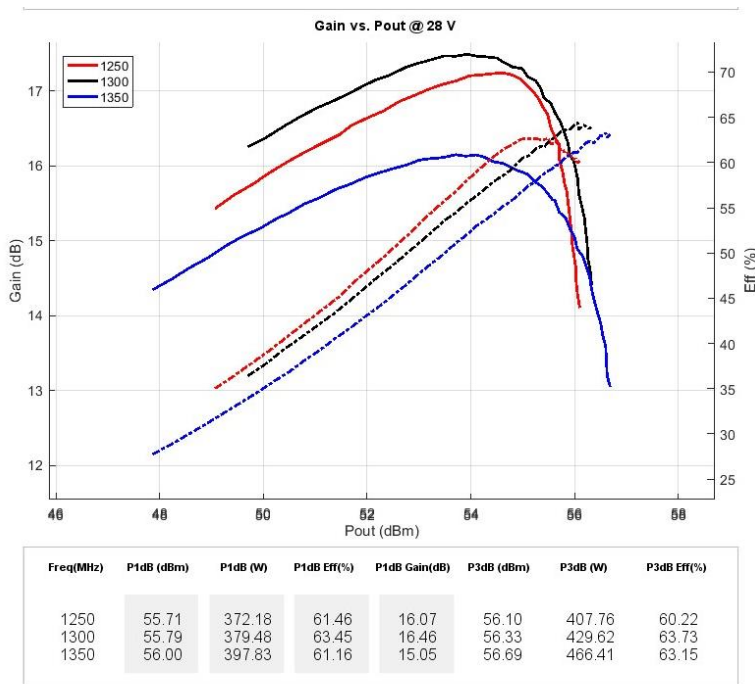
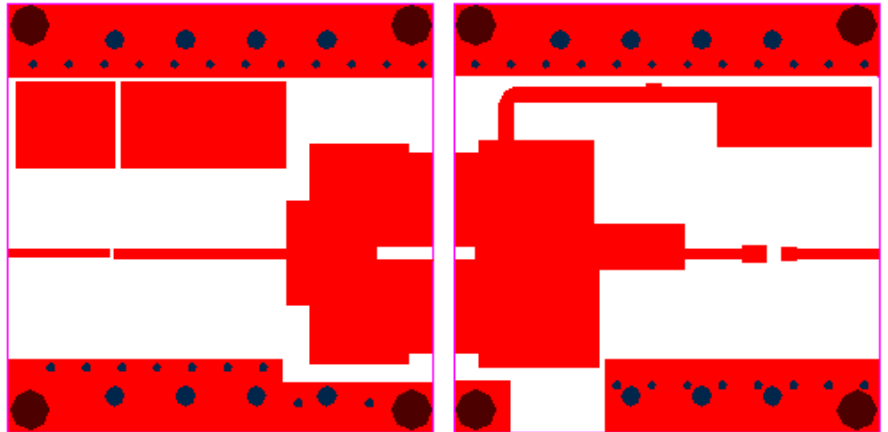


Figure 2: Test fixture photo, layout and bill of materials



PCB: 30mil RO4360 (Dielectric Constant = 6.15)

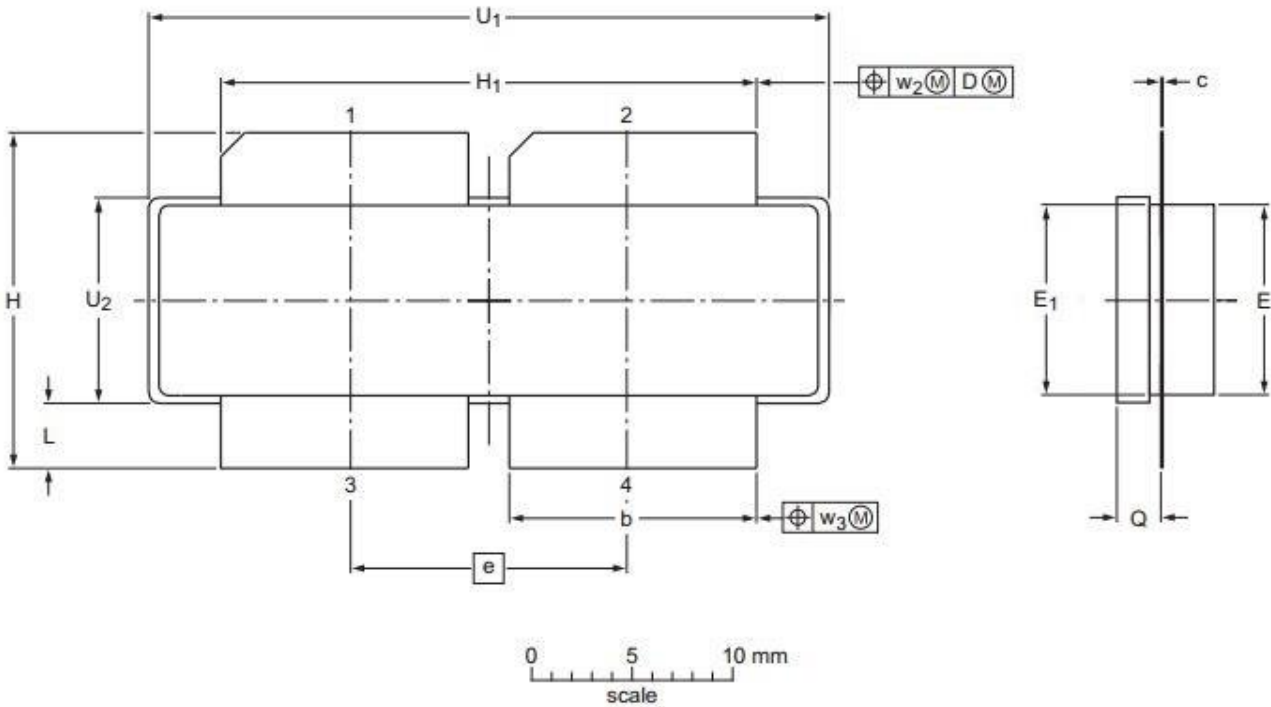
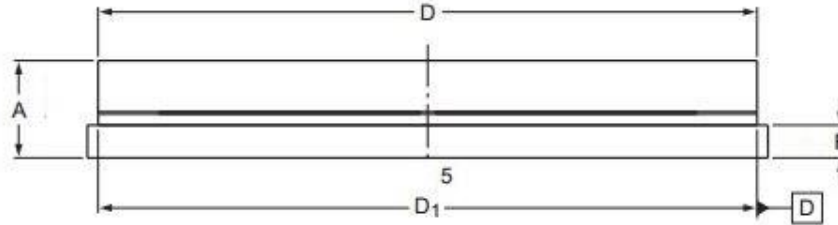
C1, C5	ATC600F 33pF
C2, C3, C6	ATC800B 33pF
C4, C7	10uF
R1	47 Ω
R2	10 Ω





Package Outline

Earless flanged ceramic package; 4 leads (1, 2—DRAIN, 3, 4—GATE, 5—SOURCE)



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₂	W ₂
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/9/19	V1	Preliminary Datasheet Creation

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